The Bulk Built In Current Sensor Approach for Single Event Transient Detection

Gilson Wirth
Departamento de Engenharia Eletrica
UFRGS - Universidade Federal do Rio Grande do Sul
Porto Alegre, Brazil
E-mail: wirth@inf.ufrgs.br

Christian Fayomi
Computer Science Department
Universite du Quebec a Montreal
Montreal, Canada
E-mail: fayomi.christian@uqam.ca

Abstract— Radiation effects, particularly Single Event Transients (SETs), are increasingly affecting the reliability of integrated circuits as device dimensions are scaling down. This paper presents the use of Bulk Built in Current Sensors (Bulk-BICS) for SET detection. The efficiency and applicability of the Bulk-BICS approach for Single Event Transient detection is demonstrated through device and circuit level simulations.

I. INTRODUCTION

Aiming to increase circuit performance, as well as to integrate more functional units into the same silicon area, scaling leads to integrated circuits made of ever shrinking devices. Power supply is also scaled down. As a consequence, the amount of electrical charge used to store information is ever decreasing. This decrease in electrical charge used to store information has made integrated circuits more susceptible to energetic particle strikes. If an energetic particle strikes a sensitive region in a semiconductor device, the resulting electron-hole pair generation injects electrical charge into the struck node. As the charge used to store information decreases, the electrical impact of the charge injected by the particle hit increases. The electrical charge injection changes the electrical voltage at the stuck node. This voltage change may be interpreted as a valid signal in the circuit, leading to a transient fault.

Built in current sensors have been used for monitoring on-chip current variations due to permanent faults, as for instance stuck at faults [3, 4]. For transient fault detection, related works have presented asynchronous BICS able to detect single event upsets (SEUs) in memories [7]. In this case, the BICS is placed on the power lines of a memory. Monitoring the current in the supply lines may be an efficient solution for sequential circuits. However, this solution does not work properly for combinational logic, because BICS connected to the power lines cannot efficiently differentiate internal signals propagating through the logic from SETs.

In order to enhance the applicability of the BICS approach and more efficiently detect SETs in integrated circuits, we...
propose a new approach able to detect transient faults based on bulk built in current sensors (bulk-BICS) [2]. In this method, a BICS is connected to the design bulk of the transistors, which increases the BICS efficiency to detect any discrepancy in the circuit internal current that may occur during a particle strike. Since under normal circuit operation the bulk current is very small if compared to the current generated by a particle strike, this approach allows the bulk-BICS to distinguish SETs from internal logic signals and consequently detect them. As a consequence, the bulk-BICS may be used to detect transient faults in digital combinatorial logic and mixed signal circuits, as well as in memories.

A simple bulk-BICS design is depicted in Figure 1. This simple design will be used to study the bulk-BICS detection mechanism in the next section. An advantage of this design is its negligible static power consumption, a key feature for VLSI. This bulk-BICS detects a SET due to an energetic particle strike at the reverse biased drain junction of PMOS transistors in the off state. The body-ties of the PMOS transistors being monitored are connected to VDD through transistor M1 of the bulk-BICS. To ensure proper connection of the body-ties to VDD, the PMOS transistor M1 has a large W/L ratio. L is the channel length and W the channel width. The PMOS transistor M2 also has a large W/L ratio, while the NMOS transistor M3 has a small W/L ratio. Under normal operation (no particle strike) the current flowing through M1 is negligible, and the gate of M2 is at VDD. As a consequence, the output Out-P of the bulk-BICS is at logic zero. If a particle strike occurs, current flows through M1, and the gate voltage of M2 slightly drops. The bulk-BICS amplifies this voltage change, and the output voltage at Out-P rises, changing its output from logic zero to logic one. Out-P may be latched and used as a flag to signal the occurrence of a SET. Error handling techniques may then be implemented at the circuit or system level, to avoid that a SET turns into a faulty behavior.

A similar design may be used to detect particle strikes at the drain of NMOS transistors in the off state [2]. Circuit and device simulations for both cases (strikes at NMOS and PMOS transistors) lead to equivalent results. To keep the paper compact, only the simulation results for particle hits at the drain of a PMOS transistor in the off state are shown here.

III. DEVICE AND CIRCUIT LEVEL SIMULATIONS

The single event transients are simulated using the Synopsys Taurus Medici package [8]. Mixed mode (level) simulations are performed using the Circuit Analysis Advanced Application Module. The charge collection and current generation mechanism is simulated in three dimensions at the device level, while the bulk-BICS response is analyzed at the circuit level.

A cross section of the struck PMOS transistor is depicted in Figure 2. The effective channel length is 0.25µm. The gate and source contacts are connected to VDD. Hence, the transistor is in the off state. The body-tie is connected to VDD through the bulk-BICS depicted in Figure 1.

To simulate the effects of a circuit attached to the drain contact, a resistor and a capacitor are connected to the drain. The drain is connected to ground through a lumped 1000 Ohms resistor, and the node capacitance of an attached circuit is simulated by a lumped capacitance of 30 fF.

These voltages reverse bias the drain-substrate junction.

For this example, power supply VDD is 2.5V, and the threshold voltages of NMOS and PMOS transistors are 0.38V and -0.38V, respectively. For the PMOS transistor simulated at the device level, the peak source/drain doping is 10^{20}/cm^3. The substrate doping is 2x10^{18}/cm^3. The peak doping of the n-type implant for the body-tie contact is also 10^{20}/cm^3.

To study the bulk-BICS detection mechanism, an 80 MeV argon ion passing through the drain of the p-channel MOSFET is simulated in three dimensions. The charge generation rate versus depth of penetration of the ion is obtained from [9].

![Figure 1. A Bulk-BICS for SET detection.](image)

![Figure 2. A cross section of the struck PMOS transistor. For the sake of simplicity only the silicon area is show. The struck drain is at top left, followed by gate and source regions. The body-tie is at top right. The flow lines indicate the total current flow in the device 8 picoseconds after the particle strike.](image)
The particle strikes at the reverse biased drain junction, at position $x=0.3\mu m$ and $z=0.0\mu m$, perpendicular to the silicon surface. During the upset process, the conductive charge track generated by the passage of the energetic particle temporarily short circuits the drain-substrate junction and pulls the drain up to the higher potential of the substrate. This voltage change at the drain node is known as single event transient at the circuit level, and may lead to circuit faulty behavior. The first 500 picoseconds (ps) of the transient response are simulated. The particle strike occurs at time $t = 0$.

Figure 3 shows the voltage at the drain contact of the struck transistor, from $t = 0$ to $t = 500$ ps. Figure 4 depicts the current at the drain and source terminals of the struck transistor, as well as the body-tie current, from $t = 0$ to $t = 80$ ps. The large spike in drain current (approximately 7 mA) is due to drift collection. The drift collection process is quickly extinguished (at about 50 ps) as all the charge in the depletion region is collected. Figure 3 shows that the voltage at the drain terminal reaches a maximum of about 1.15 Volt and slowly starts to return to ground, as the conductive channel between drain and substrate is extinguished and the drain circuit node is pulled down to ground through the 1000 Ohm resistor.

A funneling [10] behavior can be seen by examining the potential contours, as shown in Figure 5. The simulation domain extends $4\mu m$ into the silicon bulk (y-axis), although only the top $2\mu m$ is plot. Before the ion strikes, the equipotentials are parallel to the drain junction. The figure depicts the situation at 2 ps after the ion strike. The equipotentials extend into the substrate due to the voltage drop along the charge column. The funneling reaches its peak at around 5 ps, approximately the same time at which the drain current reaches its peak. Afterwards, the funnel starts to collapse and the drift current starts to decrease, as charge is swept from the depletion region at the drain. After 80 ps the depletion region at the drain is restored and only diffusion charge collection is occurring. The simulation time of 500 ps is sufficient to resolve the drift component of the charge collection process. At the end of the simulation time, there is only a small current of some microamperes at the drain terminal, due to diffusion charge collection.

Figure 6 depicts the bulk-BICS transient response, from time $t = 0$ to time $t = 500$ ps. The voltages at the body-tie contact and at the bulk-BICS output are plotted. The output of the bulk-BICS crosses the logical threshold, changing its output state from logical zero to logical one. Since the transistor M2 has much larger W/L ratio than M3, the output
quickly changes from logical zero to logical one. After reaching its peak value, the output slowly returns to zero, due to the current conducted through M3. Out-P may be latched and used as a flag to signal the occurrence of a SET. Techniques to mitigate the effects of a SET may then be implemented at the circuit or at the system level, improving product reliability. For instance, if the bulk-BICS is used to monitor the circuitry of a microprocessor with recomputing and pipeline refreshing capabilities, Out-P may be used to signal the need for recomputation or pipeline refreshing. The bulk-BICS approach may help improving high-level fault-tolerance methods based on fault detection and correction.

To verify the impact of body-tie spacing on bulk-BICS detection, the distance between body-tie and struck transistor was varied. If the body-tie is placed 16 µm apart from the struck transistor, the peak current at the body-tie decreases by 21%, and the bulk-BICS properly detects the particle hit. The total charge injected at the body-tie contact (integration of current over time) changes less than 10%. The change in the current and voltage waveforms at the drain contact is negligible.

A single bulk-BICS can be used to monitor several transistors. This can be done by connecting the input of the bulk-BICS (“To Body-Tie” contact) to several body-ties. However, since this increases the capacitance at this node, there is a limit for the maximum number of transistors that can be monitored by a single bulk-BICS, as discussed in [2]. The maximum number of transistors that can be monitored by a single bulk-BICS depends on technology node and bulk-BICS design. In [2], two bulk-BICS are used to detect SETs in up to 128 SRAM memory cells.

With scaling, node capacitances and supply voltages decrease, and integrated circuits become susceptible to SETs due to strikes by lower energy particles. Particle hits by ions of higher and lower linear energy transfer (LET) have also been simulated, using the mixed mode simulation methodology described here. Particles that deposit more charge result in an increased voltage perturbation at the drain terminal, and induce a higher body tie current. The capacitive and resistive loading effects at the drain contact have also been analyzed. As discussed in [2], the bulk-BICS sensitivity may be adjusted by proper sizing of transistors M1, M2 and M3, or by using improved bulk-BICS designs. The mixed mode simulations run confirm that the bulk-BICS approach is efficient in detecting single event transients.

IV. CONCLUSION.

The efficiency of the Bulk Built In Current Sensor Approach for Single Event Transient Detection is validated by device simulation. It is shown that the bulk-BICS properly detects the energetic particle strike, presenting an efficient technique to improve the reliability of integrated circuits against radiation effects.

Future work will focus on the design, fabrication and test of a chip with an integrated bulk-BICS under energetic particle bombardment (irradiation).

Figure 6. Voltage at the body-tie contact, as well as voltage at the output Out-P of the bulk-BICS. Squares (●): Voltage at the body-tie contact; Circles (○): Voltage at Out-P.

REFERENCES